MAKE-UP EXAM

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BBEE103/203

First/Second Semester B.E./B.Tech. Degree Examination, Nov./Dec. 2023
Basic Electronics for EEE Stream

Time: 3 hrs. Max. Marks: 100

Note: **1.** ***Answer any FIVE full questions, choosing ONE full question from each module.***
2. ***M : Marks , L: Bloom's level , C: Course outcomes.***
3. ***Assume any missing data suitably.***

		Module – 1	M	L	C
Q.1	a.	With the help of neat circuit diagram and waveform, explain the working of full wave, rectifier with center tapped transformer.	8	L2	CO1
	b.	Explain the forward and reverse characteristics of semiconductor diode.	6	L2	CO1
	c.	A Zener regulator has the following data : V_i = 16V, V_0 = 6V, $I_{L(max)}$ = 60mA, Z_z = 7Ω, R = 150Ω. Calculate line regulation and ripple rejection ratio.	6	L3	CO1
		OR			
Q.2	a.	Describe the working of a capacitor filter for a half wave rectifier with a neat circuit diagram and necessary waveforms.	8	L3	CO1
	b.	What is a DC load line? With the help of neat circuit diagram and waveform, explain the procedure of constructing a DC load line for a semiconductor diode.	8	L3	CO1
	c.	Define : i) Line regulation ii) Load regulation.	4	L2	CO1
		Module – 2			
Q.3	a.	Explain the construction and working of n-channel JFET.	8	L3	CO2
	b.	Draw and explain output characteristics of CE configuration.	6	L3	CO2
	c.	For the base bias circuit, R_c = 12KΩ, R_B = 470KΩ, V_{cc} = 20V and V_{BE} = 0.7V. Construct the DC load line and indicate the values.	6	L3	CO2
		OR			
Q.4	a.	Explain the construction and working of n-enhancement MOSFET.	8	L3	CO2
	b.	Explain the common base output characteristics.	8	L2	CO2
	c.	Describe how a transistor can be used as a voltage amplifier.	4	L2	CO2
		Module – 3			
Q.5	a.	Explain the block diagram of a typical op-amp.	8	L2	C2
	b.	Explain the following terms : i) Input offset current ii) Input bias current iii) CMRR iv) Slew rate v) Input offset voltage vi) Voltage gain.	6	L2	C2

	c.	Construct an adder circuit using op-amp to obtain an output voltage of $V_0 = -[2V_1 + 3V_2 + 5V_3]$	6	L3	CO2
		OR			
Q.6	a.	Describe an integrating amplifier using an op-amp in an investing configuration.	8	L2	CO2
	b.	Explain basic differential amplifier using op-amp.	8	L2	CO2
	c.	List the characteristics of an ideal op-amp.	4	L2	CO2
		Module – 4			
Q.7	a.	Explain full adder circuit with truth table. Realize the circuit for sum and carry using basic gates.	8	L2	CO3
	b.	Explain the Boolean function $F = A + \overline{B}C$ in a sum of minterms.	6	L3	CO3
	c.	Convert the following i) $(10AB)_{16} = (\ ?\ )_{10}$ ii) $(240)_{10} = (\ ?\ )_2$ iii) $(1234.56)_8 = (\ ?\ )_{10}$	6	L2	CO3
		OR			
Q.8	a.	Simplify the following Boolean expressions : i) $f(w, x, y, z) = x + xyz + \overline{x}yz + wx + \overline{w}x + \overline{x}y$ ii) $f = \overline{(A+\overline{B}+C)(\overline{A}+\overline{B}+C)+(\overline{A}+B)}$	8	L3	CO3
	b.	Explain SOP and POS with examples.	6	L3	CO3
	c.	Implement half adder using basic gates.	6	L2	CO3
		Module – 5			
Q.9	a.	With suitable diagram, explain working of Linear variable differential transducer.	8	L2	CO4
	b.	What is modulation? Describe the need of modulation in communication systems.	6	L2	CO4
	c.	Write short note on piezoelectric transducer.	6	L2	CO4
		OR			
Q.10	a.	Explain the working of potentiometric resistive transducer with neat diagram.	8	L2	CO5
	b.	Explain the various blocks involved in an electrical communication systems.	6	L2	CO5
	c.	A parallel plate capacitive transducer has a plate area ($\ell \times w$) = 40mm * 40mm) and plate spacing (d) = 0.5mm. Calculate the device capacitance and the displacement that causes the capacitance to change by 5pF. Also determine the transducer sensitivity.	6	L3	CO5

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